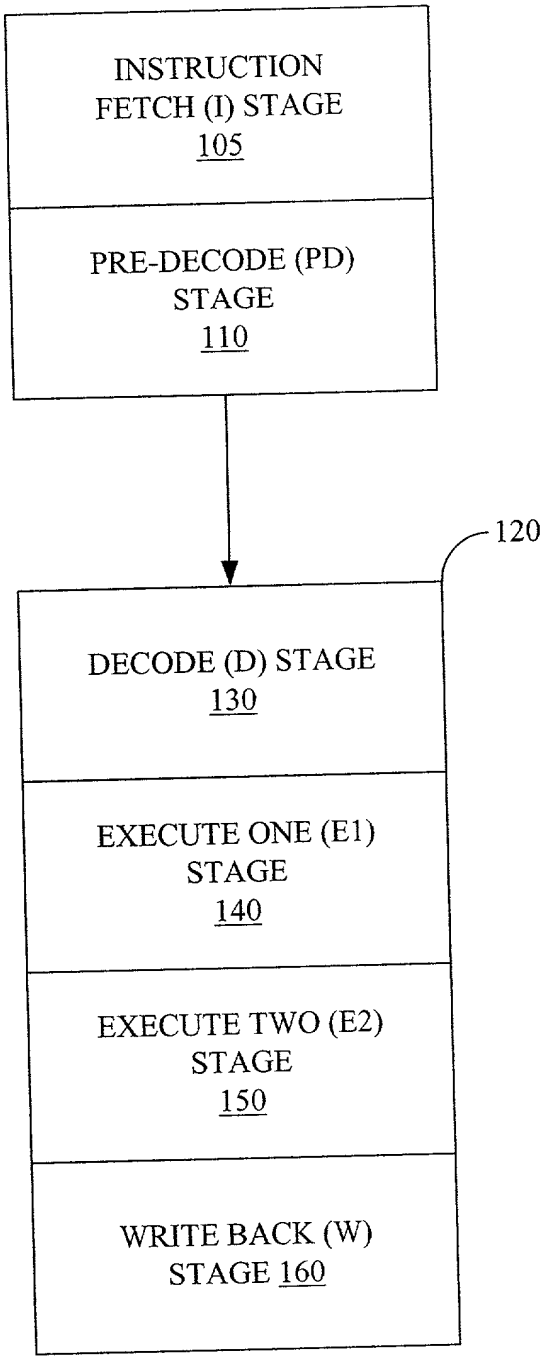


FIGURE 1 (Prior Art)

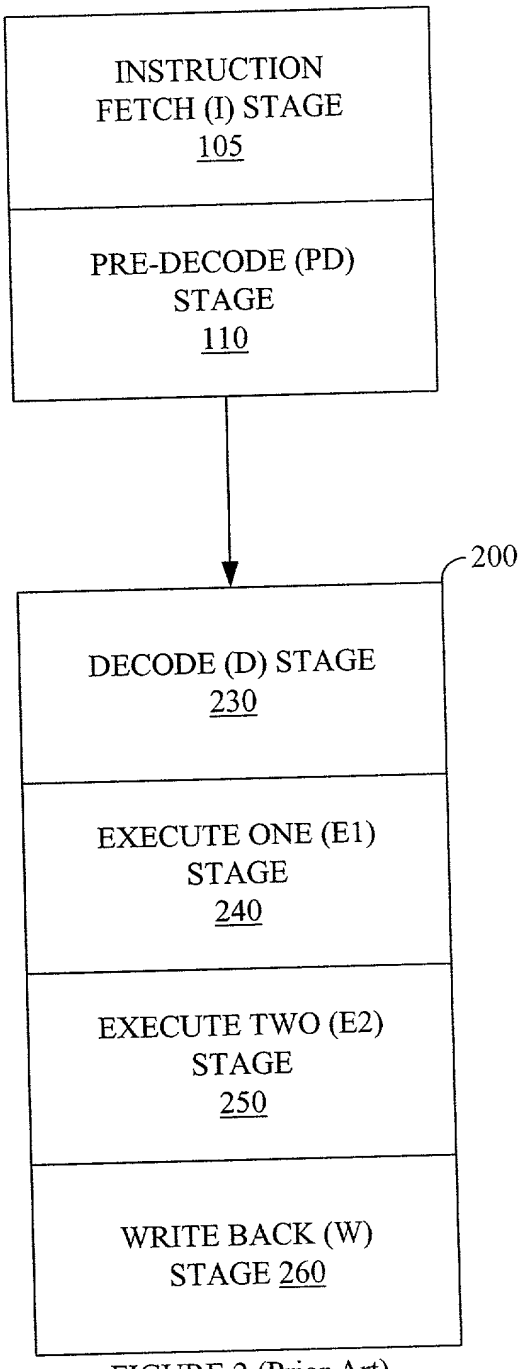


FIGURE 2 (Prior Art)

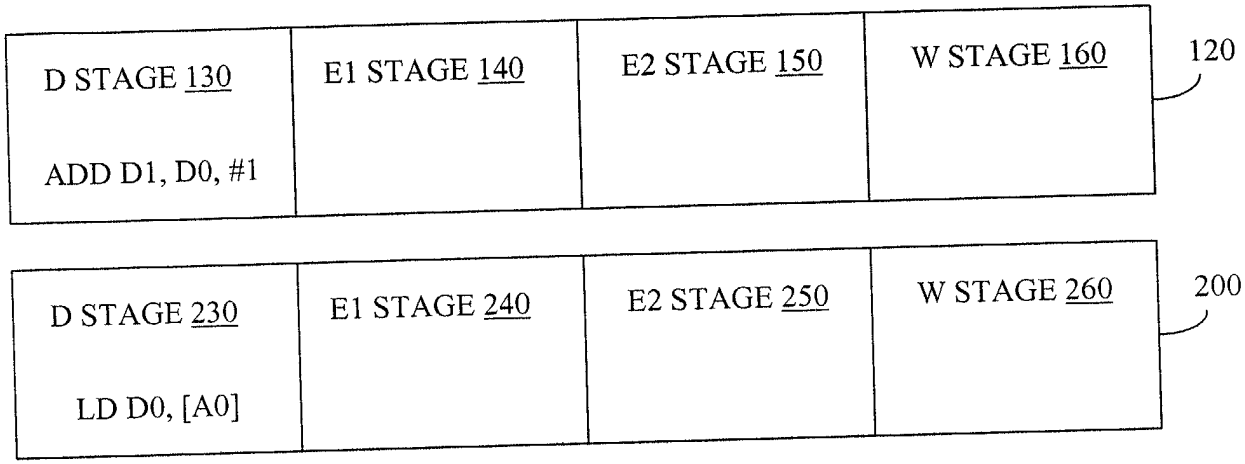


Figure 3(a)

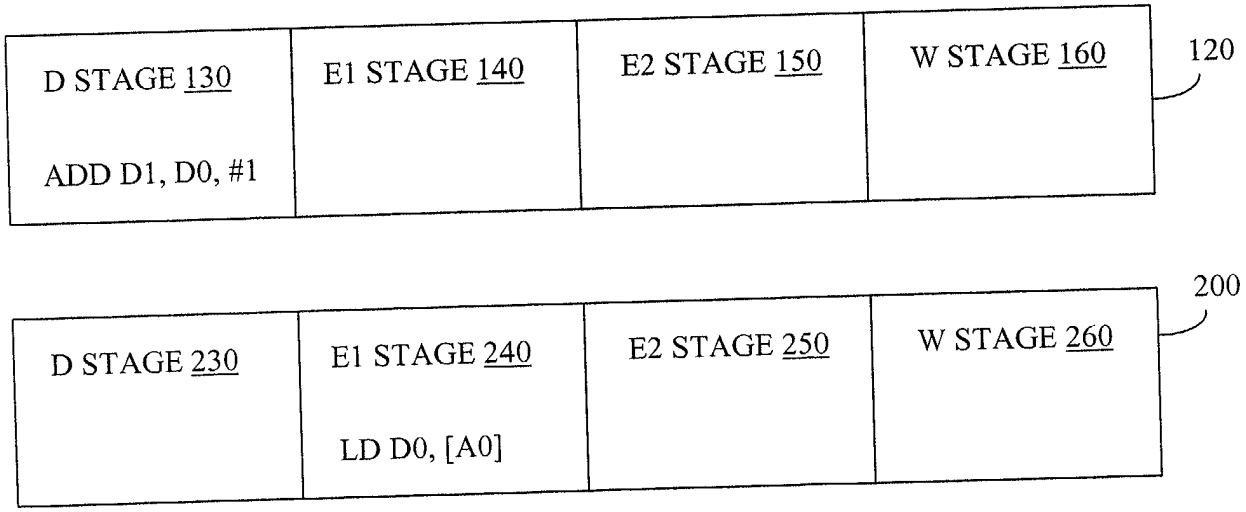


Figure 3(b)

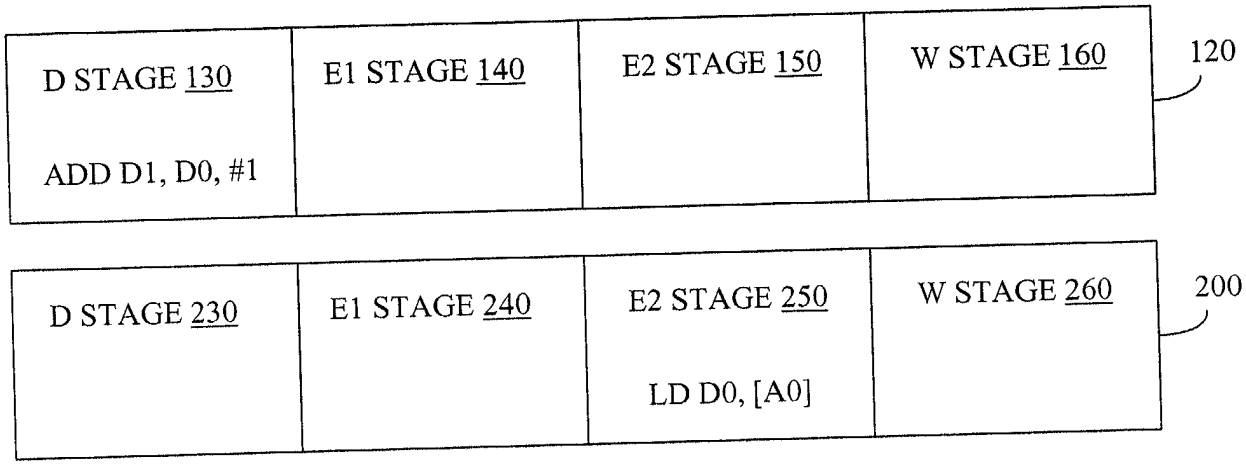


Figure 3(c)

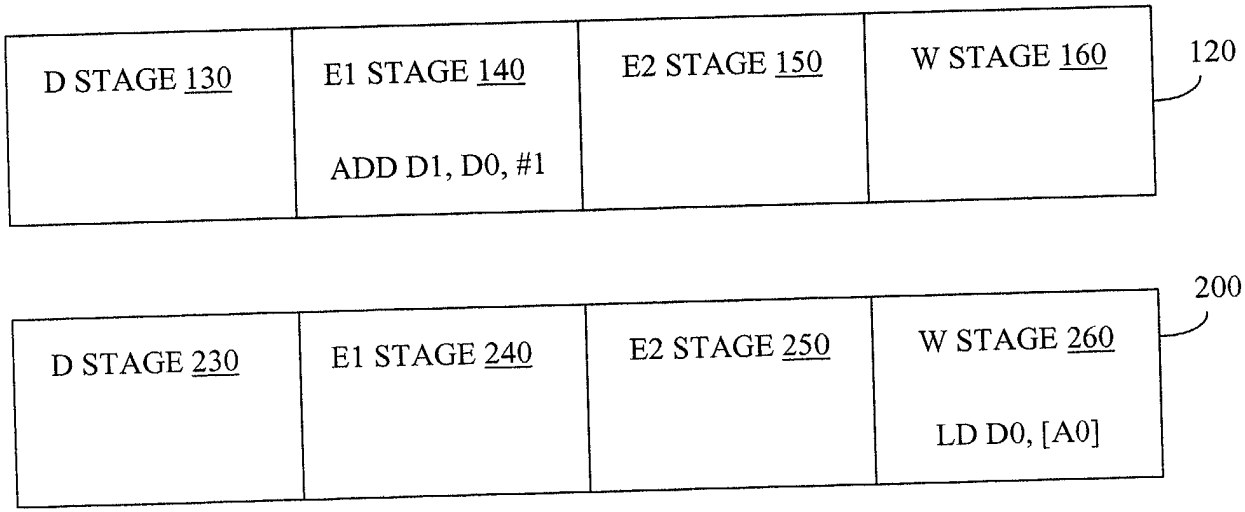


Figure 3(d)

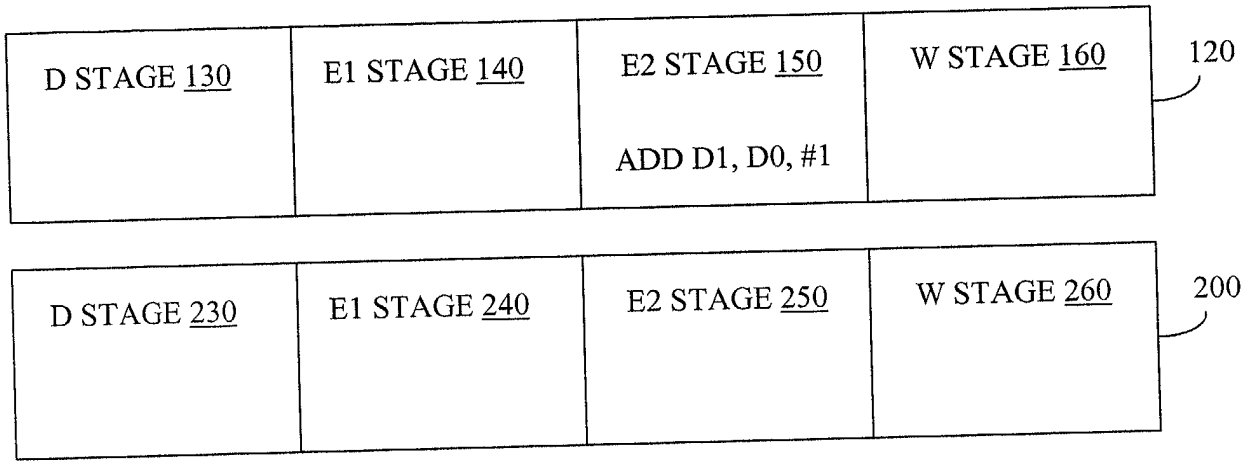


Figure 3(e)

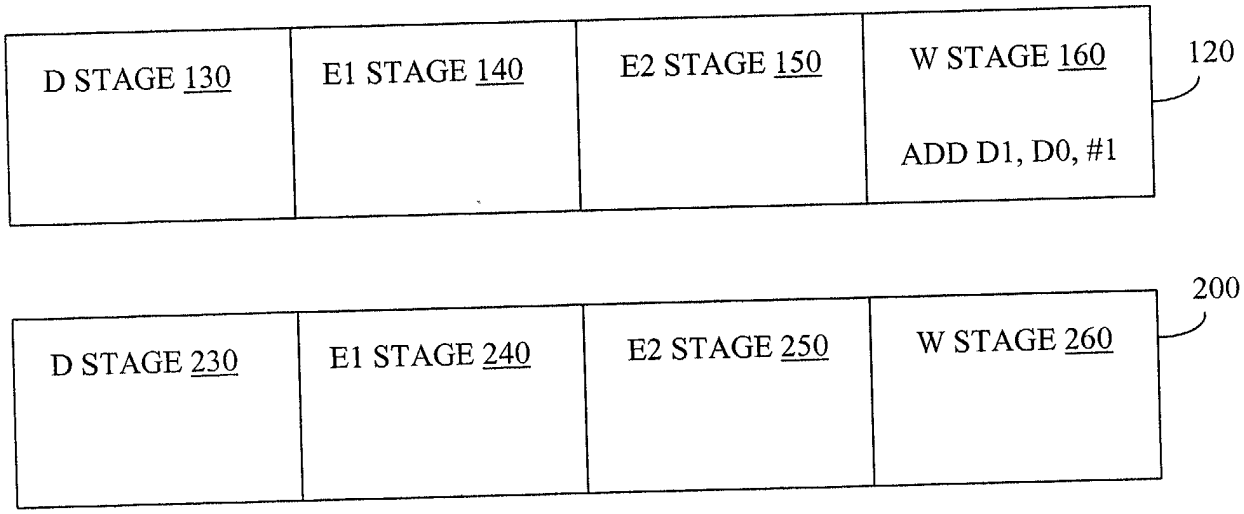


Figure 3(f)

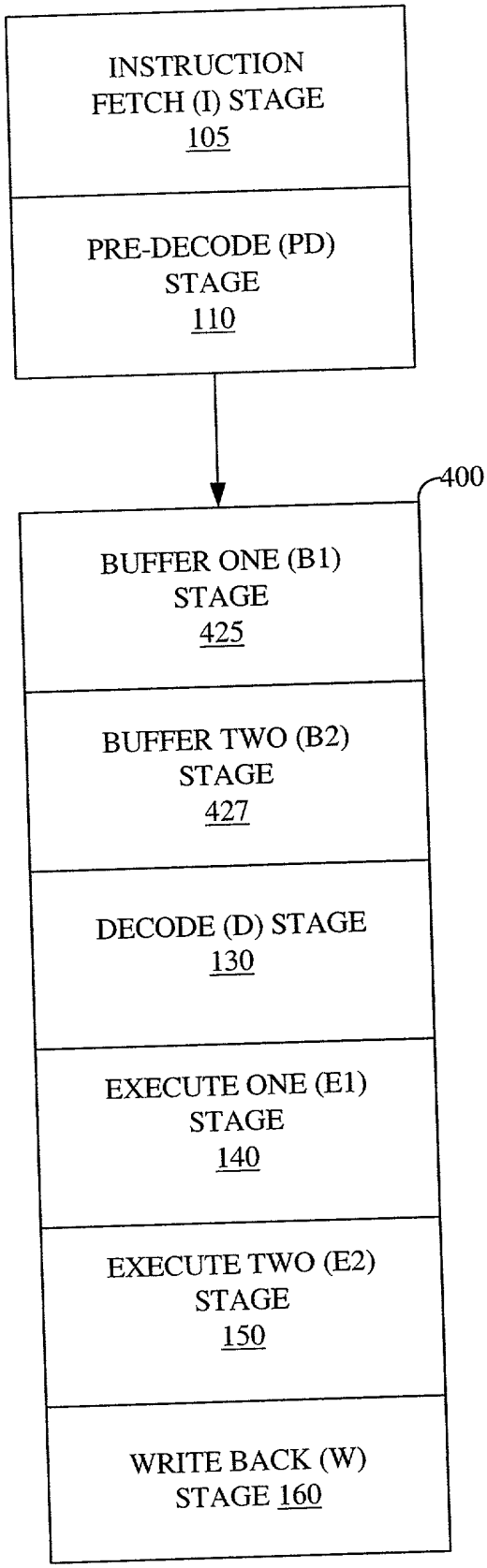


FIGURE 4 (Prior Art)

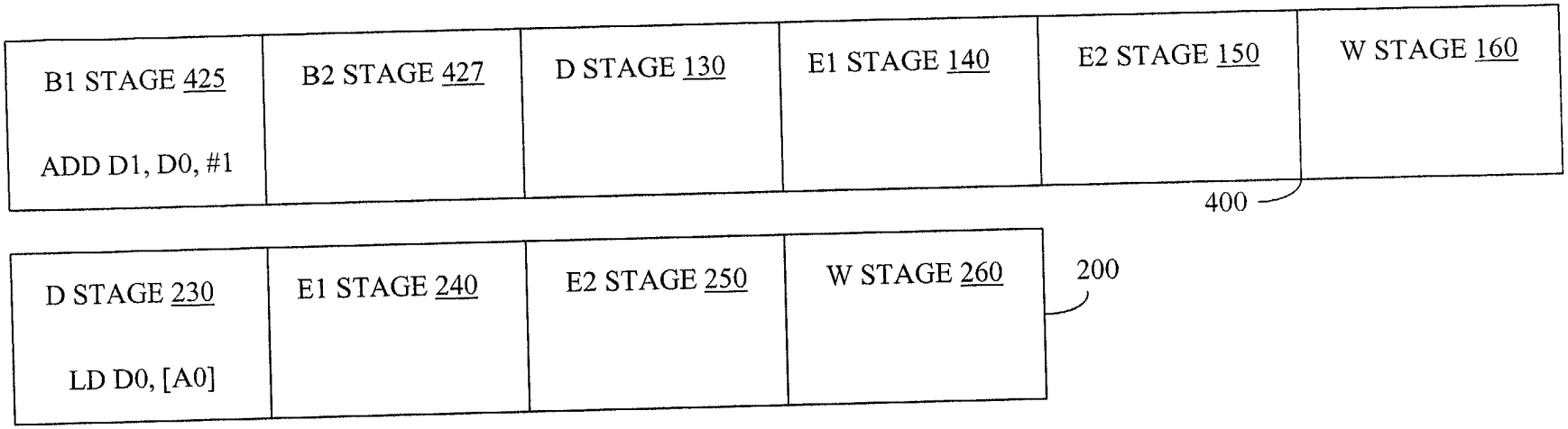


Figure 5(a)

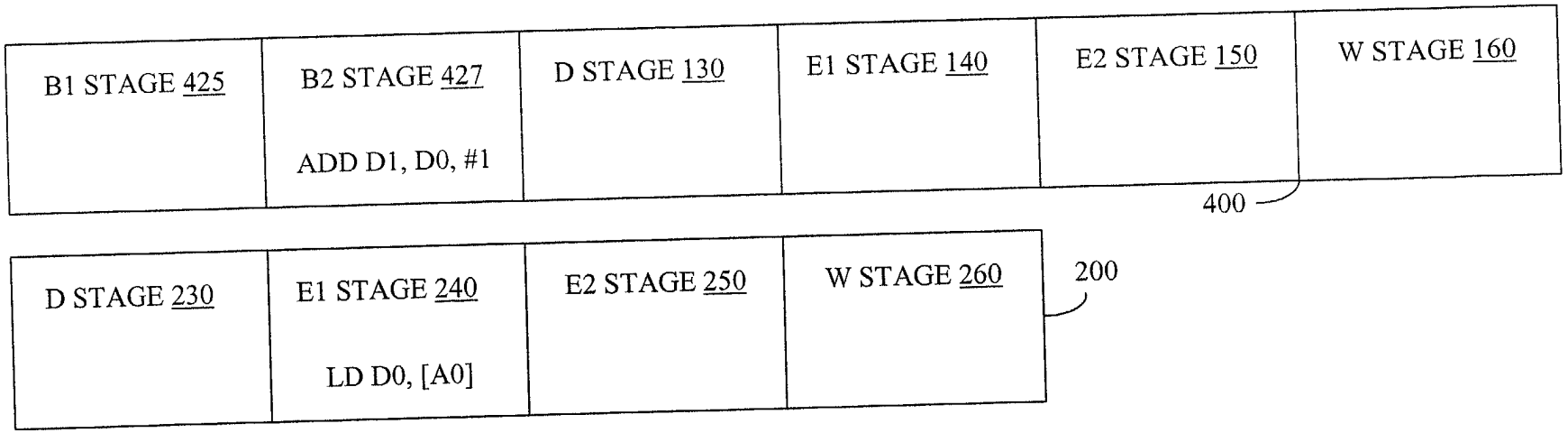


Figure 5(b)

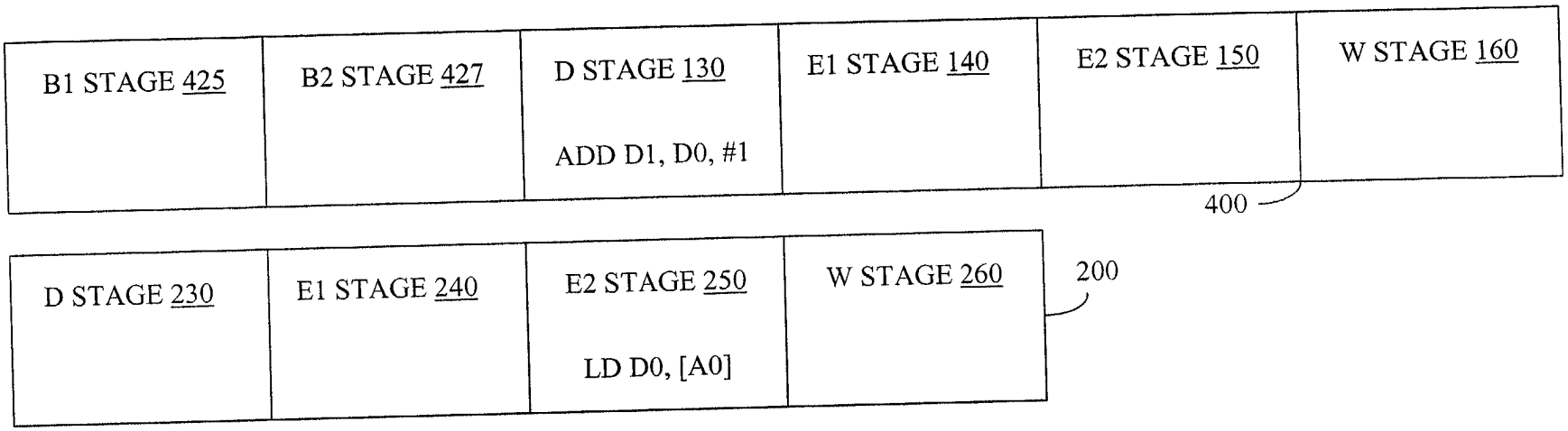


Figure 5(c)

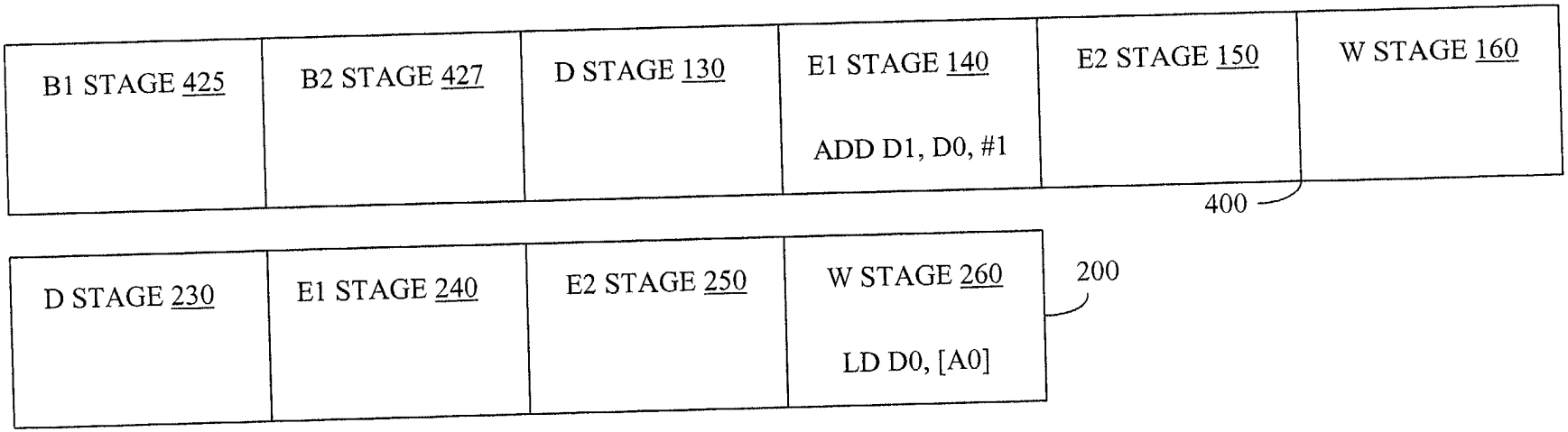
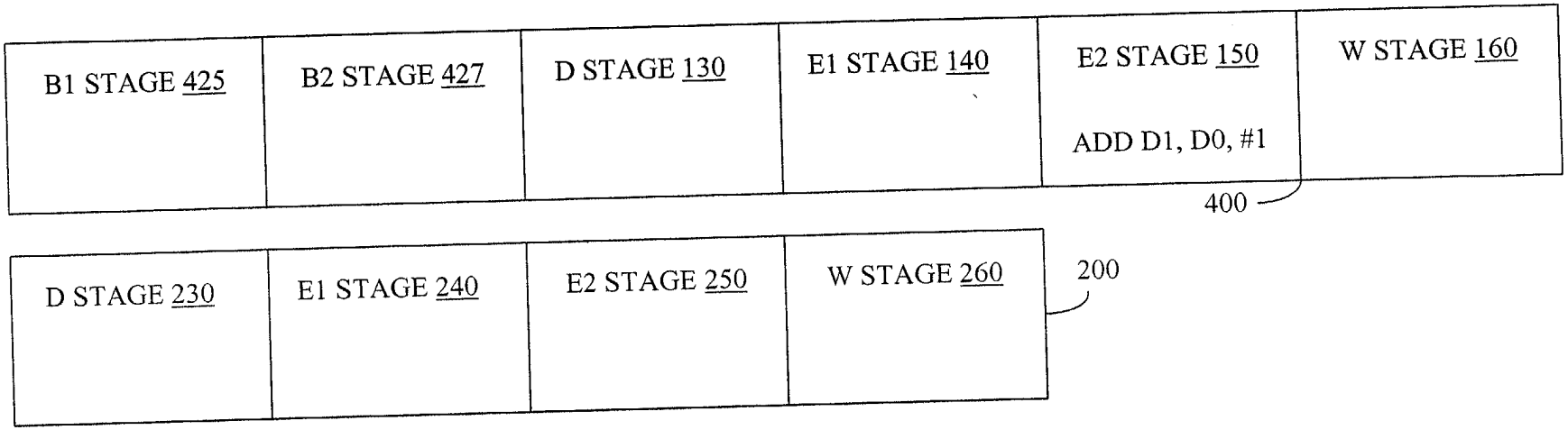


Figure 5(d)



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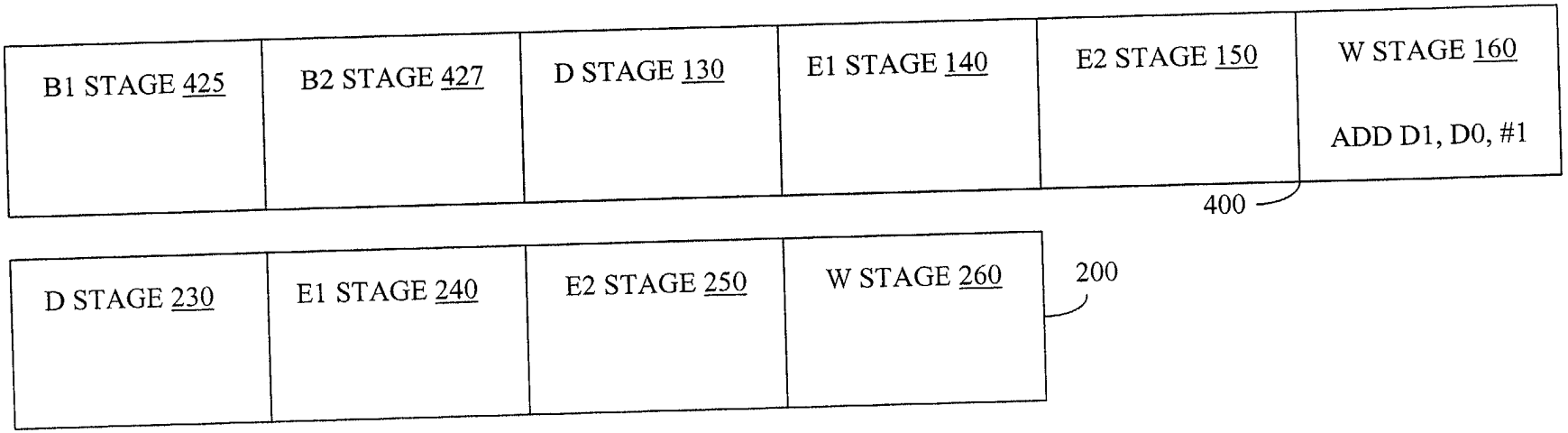

Figure 5(f)

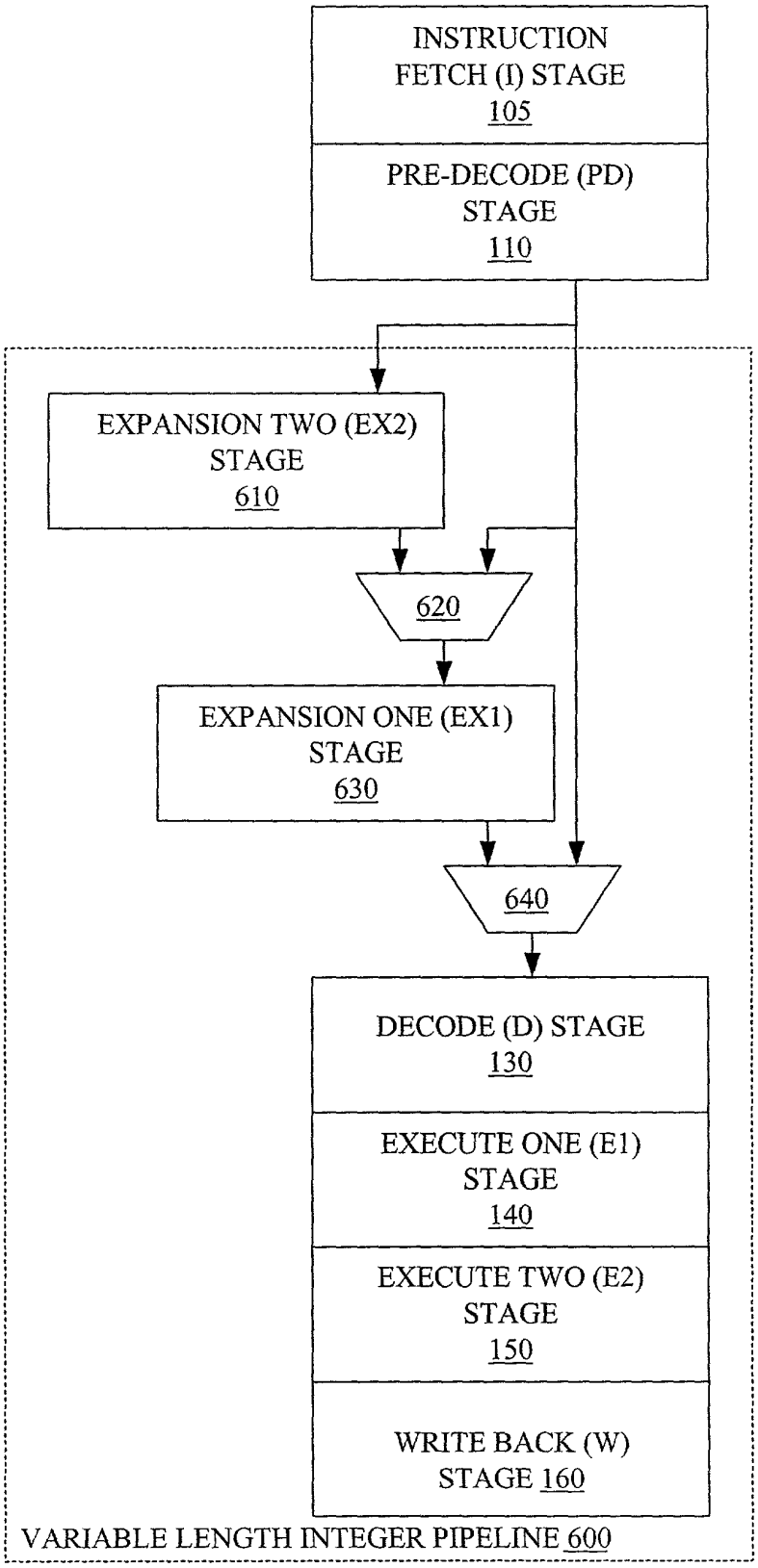
INSTRUCTION FETCH (I) STAGE 105
PRE-DECODE (PD) STAGE 110
EXPANSION TWO (EX2) STAGE 610
620
EXPANSION ONE (EX1) STAGE 630
640
DECODE (D) STAGE 130
EXECUTE ONE (E1) STAGE 140
EXECUTE TWO (E2) STAGE 150
WRITE BACK (W) STAGE 160
VARIABLE LENGTH INTEGER PIPELINE 600

FIGURE 6

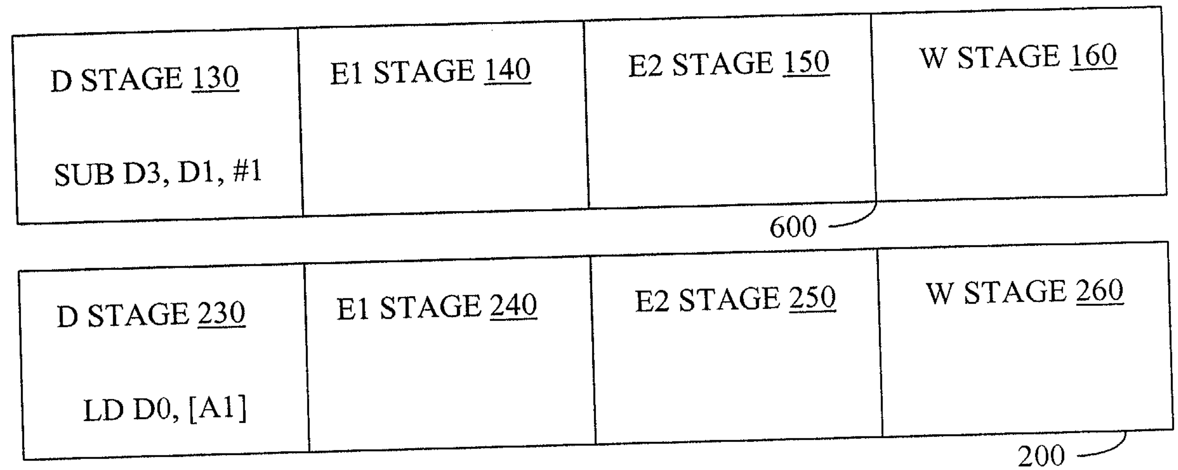

Figure 7(a)

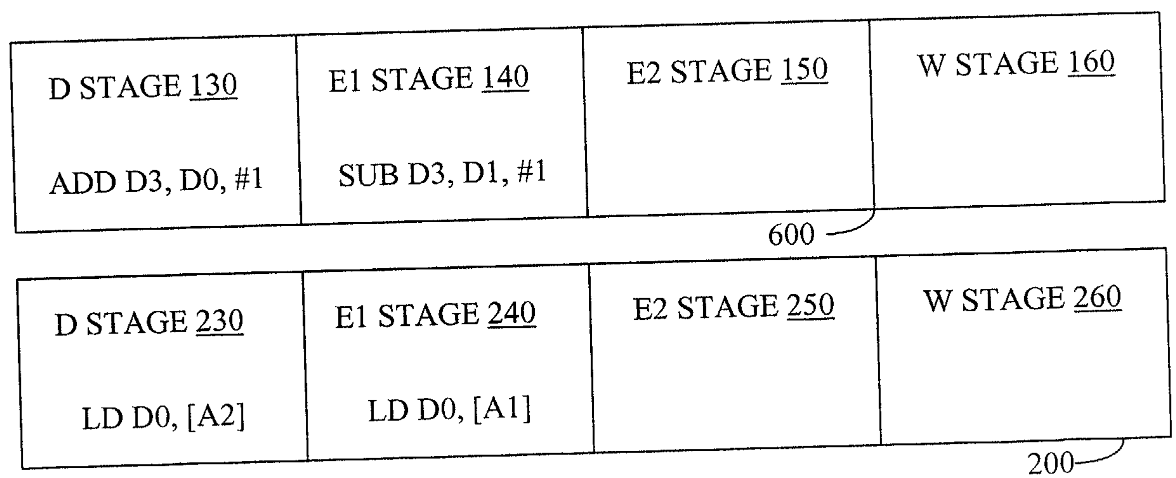

Figure 7(b)

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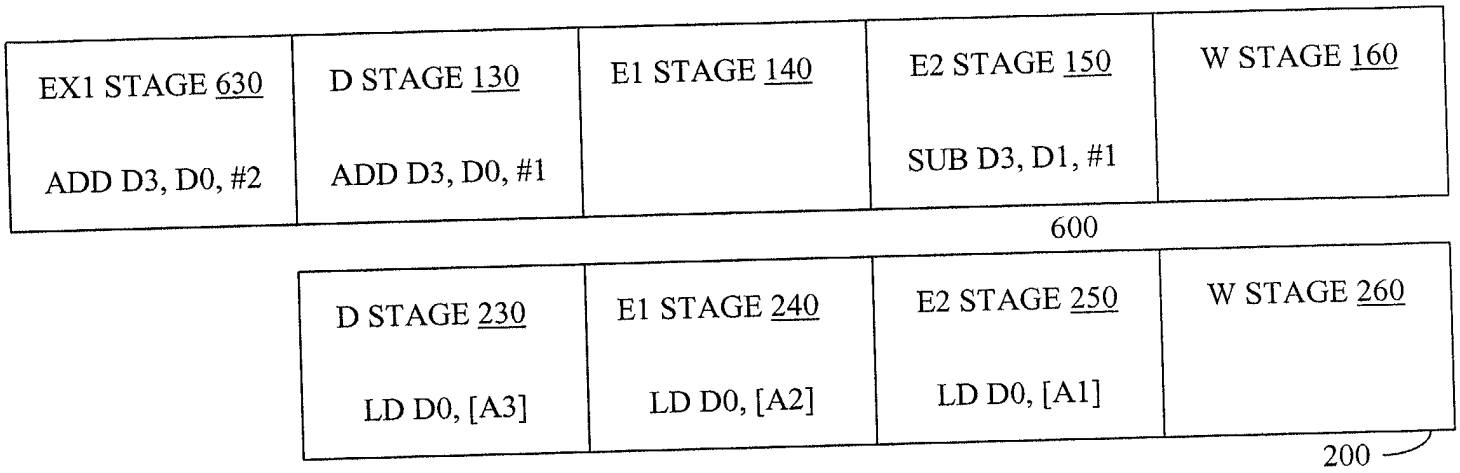


Figure 7(c)

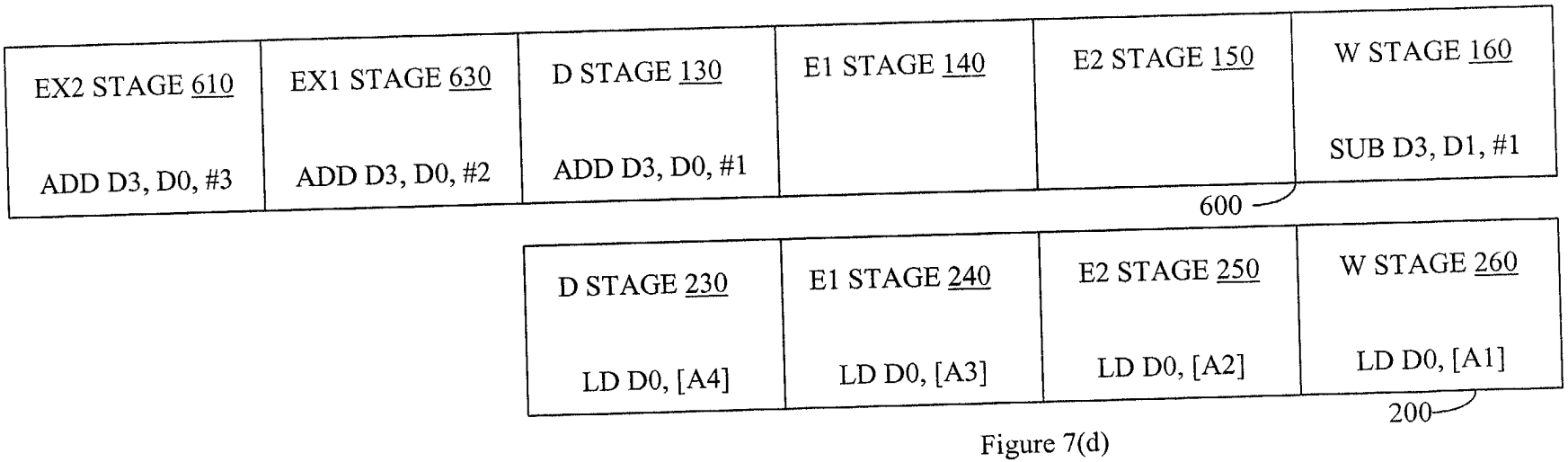
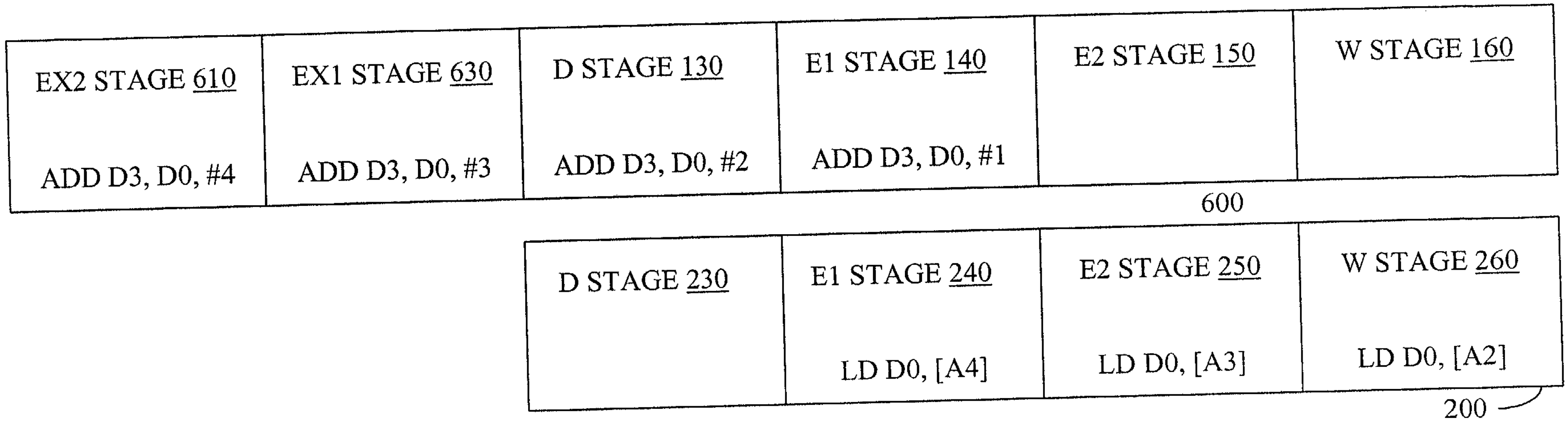


Figure 7(d)



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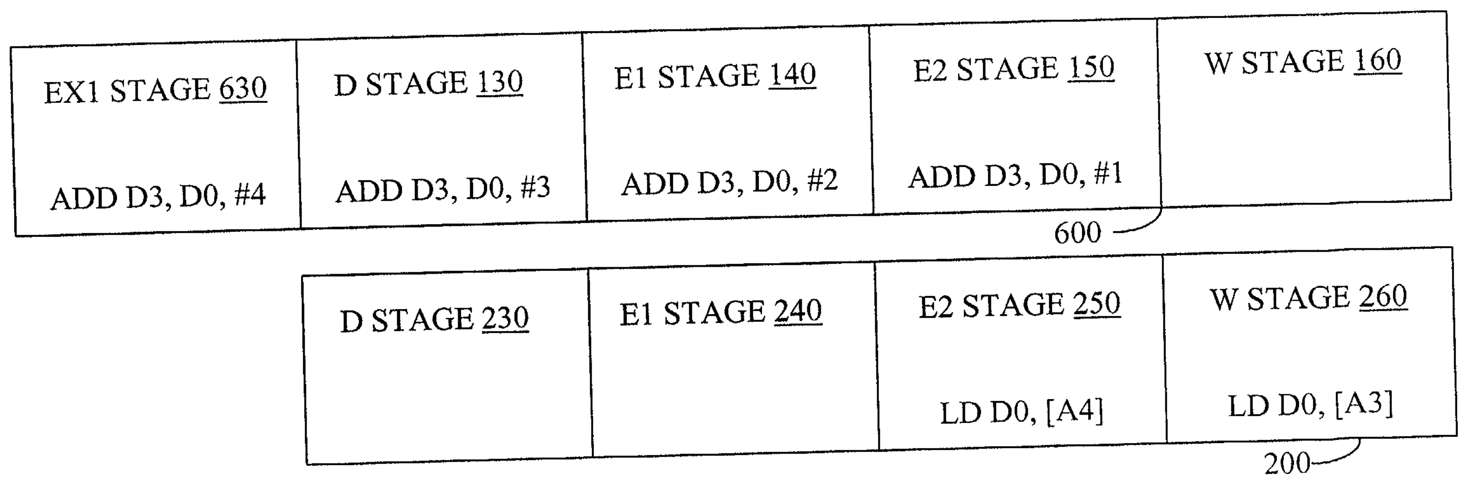

Figure 7(f)

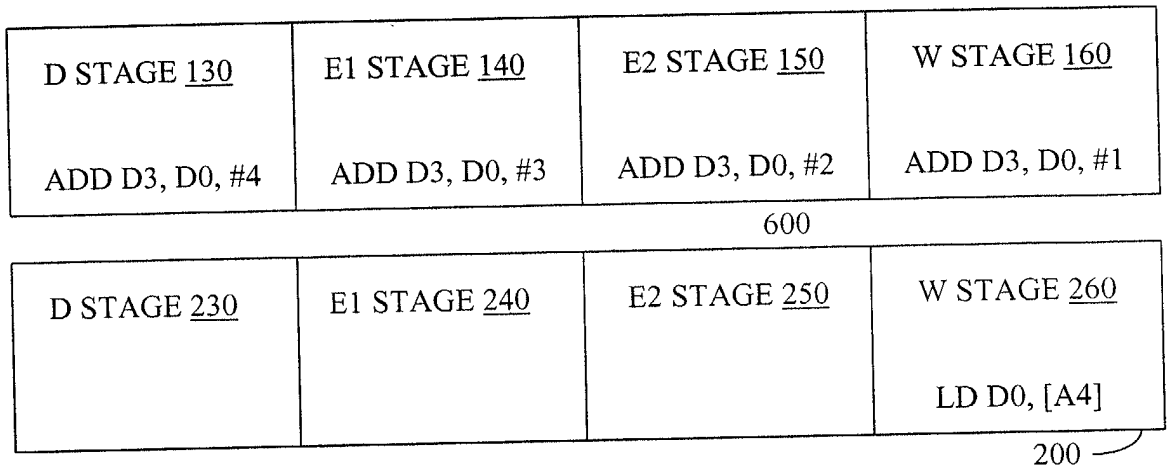

Figure 7(g)

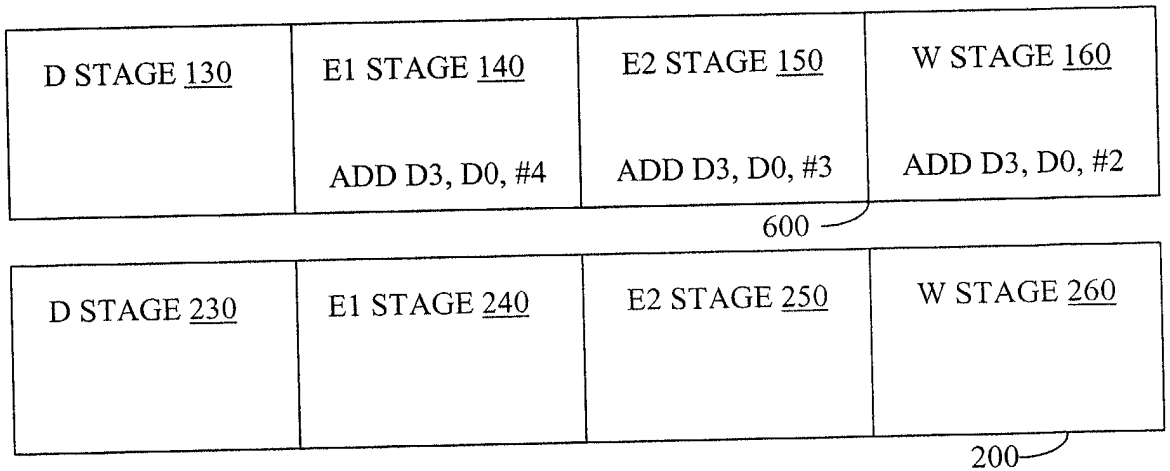

Figure 7(h)

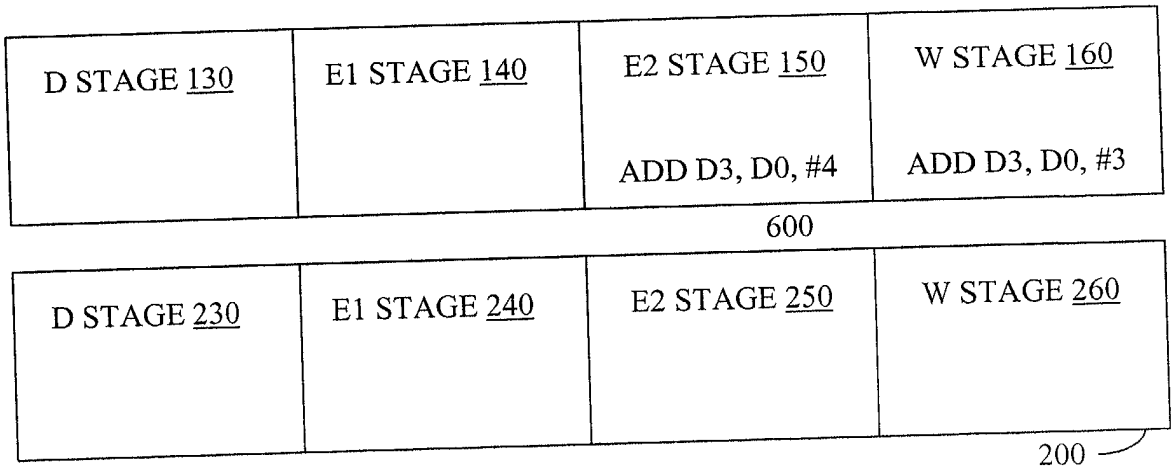

Figure 7(i)

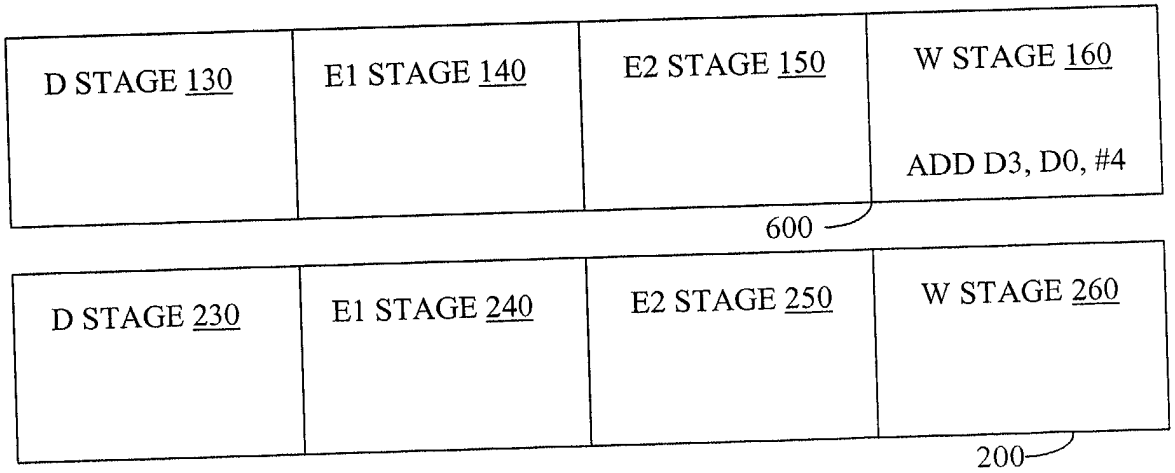

Figure 7(j)